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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Reissue Patent Application:

Applicant	:	Todd A. Merritt
Assignee	:	Micron Technology, Inc.
Filed	:	Concurrently herewith
For	:	OUTPUT BUFFER HAVING INHERENTLY PRECISE DATA MASKING
Docket No.	:	500345.02

Corresponding Issued U.S. Patent:

Patent No.	:	5,983,314
Issued:	:	November 9, 1999
Application No.	:	08/898,177
Filing Date	:	July 22, 1997
Examiner	:	Denise Tran
Art Unit	:	2752

BOX REISSUE PATENT APPLICATION
Commissioner of Patents
Washington, DC 20231

PRELIMINARY AMENDMENT

Sir:

Please accept the request for a reissue of U.S. Patent No. 5,983,314, filed herewith. Prior to conducting the examination of the reissue claims, please amend the reissue application as follows:

Please add the following new claims 54-78:

- - 54. A method of masking data coupled through a data output buffer responsive to a data mask signal applied to the output buffer, the output buffer having first and second stages connected in series with each other, the method comprising:

applying complimentary first and second data signals to respective first and second input terminals of the first stage;

selectively applying either an inactive data mask signal or an active data mask signal to the first stage responsive to an edge of a clock signal;

coupling the first and second input terminals to respective first and second output terminals of the first stage when the data mask signal applied to the first stage is inactive;

applying respective predetermined signals to the first and second output terminals of the first stage when the data mask signal applied to the first stage is active;

coupling the first and second output terminals of the first stage to respective input terminals of the second stage;

applying a data output signal to an output terminal of the second stage corresponding to the complimentary first and second data signals when the respective predetermined signals are not being applied to the first and second input terminals of the second stage; and

tri-stating the output terminal of the second stage when the respective predetermined signals are being applied to the first and second input terminals of the second stage.

55. The method of claim 54 wherein the respective predetermined signals applied to the first and second output terminals of the first stage are any signals that are not complimentary to each other.

56. The method of claim 55 wherein the predetermined signals correspond to logic "1".

57. The method of claim 54 wherein the coupling of the first and second input terminals to the respective first and second output terminals of the first stage is delayed in time so that the complimentary first and second data signals are stored in the first stage for a predetermined time.

58. A method of selectively masking complimentary read data signals responsive to a data mask signal, comprising:

generating first and second coded read data signals corresponding to the complimentary read data signals, respectively, in the absence of the data mask signal;

coding the first and second coded read data signals in a predetermined manner responsive to the data mask signal;

generating on a data output terminal an output signal having a value determined by the first and second coded read data signals if the coded read data signals are not coded in the predetermined manner, the output signal being generated by coupling the data output terminal to a first voltage if the first coded read data signal has a first value, and coupling the data output terminal to a second voltage if the second coded read data signal has the first value; and

placing the data output terminal at a high impedance by isolating the data output terminal from the first and second voltages if the coded read data signals are coded in the predetermined manner.

59. The method of claim 58 wherein the predetermined manner of coding is for the coded read data signals to have the same value.

60. A method of masking data coupled through a data output buffer responsive to a data mask signal applied to the output buffer, the output buffer having first and second stages connected in series with each other, the method comprising:

applying complimentary first and second data signals to respective first and second input terminals of the first stage;

selectively applying either an inactive data mask signal or an active data mask signal to the first stage;

coupling the first and second input terminals to respective first and second output terminals of the first stage when the data mask signal is inactive;

applying respective predetermined signals to the first and second output terminals of the first stage when the data mask signal is active;

coupling the first and second output terminals of the first stage to respective input terminals of the second stage;

applying a data output signal to an output terminal of the second stage corresponding to the complimentary first and second data signals when the respective predetermined signals are not being applied to the first and second input terminals of the second stage; and

tri-stating the output terminal of the second stage when the respective predetermined signals are being applied to the first and second input terminals of the second stage.

61. The method of claim 60 wherein the respective predetermined signals applied to the first and second output terminals of the first stage are any signals that are not complimentary to each other.

62. The method of claim 61 wherein the predetermined signals correspond to logic “1”.

63. The method of claim 60 wherein the coupling of the first and second input terminals to the respective first and second output terminals of the first stage is delayed in time so that the complimentary first and second data signals are stored in the first stage for a predetermined time.

64. A method of selectively masking complimentary read data signals responsive to a data mask signal, comprising:

generating coded read data signals corresponding to the complimentary read data signals in the absence of the data mask signal;

generating coded read data signals coded in a predetermined manner responsive to the data mask signal;

generating on a data output terminal an output signal having a value corresponding to the coded read data signals if the coded read data signals are not coded in the predetermined manner; and

placing the data output terminal at a high impedance if the coded read data signals are coded in the predetermined manner.

65. The method of claim 64 wherein the predetermined manner of coding is for the coded read data signals to have the same value.

66. An output buffer, comprising:

a data coder having complimentary data input terminals, a pair of data read output terminals, and a data mask control terminal, the data coder generating at respective first and second data read output terminals complimentary data read output signals corresponding to complimentary data input signals applied to respective data input terminals when an inactive data mask control signal is applied to the data mask control terminal, the data coder generating at the respective first and second data read output terminals data read output signals having predetermined values when an active data mask control signal is applied to the data mask control terminal; and

an output stage having respective input terminals coupled to the first and second data read output terminals of the data coder, the output stage generating a data output signal at an output terminal that corresponds to the data read output signals from the data coder when the data read output signals do not have the predetermined values, the output stage producing a relatively

high impedance at the data output terminal when the data read output signals have the predetermined values.

67. The output buffer of claim 66 wherein the predetermined values of the data read output signals are any values in which the data read output signals at the respective first and second data read output terminals have the same value.

68. The output buffer of claim 67 wherein the predetermined values of the data read output signal correspond to logic "1".

69. The output buffer of claim 66 wherein the output stage comprises a logic circuit that causes the data output signal to have a first logic level responsive to one of the data read output signals having a first predetermined logic level, that causes the data output signal to have a second logic level responsive to the other of the data read output signals having a second predetermined logic level, and that causes the data output terminal to have the relatively high impedance responsive to both of the read output signals having other than the first and second predetermined logic levels.

70. A dynamic random access memory having an address bus, at least one data bit line, and a plurality of control lines, comprising:

an array of memory cells having a plurality of memory cells, a plurality of row lines, a plurality of complimentary digit lines, and a pair of complimentary data ports;

a row address decoder coupled to the address bus, the row address decoder adapted to receive a row address on the address bus and activate a corresponding one of the row lines of the array;

a column address decoder coupled to the address bus, the column address decoder adapted to receive a column address on the address bus and couple a corresponding pair of complimentary digit lines of the array to respective data ports of the array; and

a data path coupled between the data ports and a data bit line, the data path including a input data buffer adapted to convert an input data bit applied to the data bit line to a corresponding input data signal and a complimentary input data signal, and to apply the input data signals to respective data ports of the array, and an output data buffer adapted to convert an output data signal and a complimentary output data signal applied to respective data ports of the array to an output data bit corresponding to the output data signal, and to apply the output data signal to the data bit line, the output buffer comprising:

a data coder having complimentary data input terminals coupled to the data ports of the array to receive respective output data signals, a pair of data output terminals, and a data mask control terminal, the data coder generating at respective first and second data output terminals complimentary data read output signals corresponding to complimentary data output signals applied to the respective input terminals of the data coder when an inactive data mask control signal is applied to the data mask control terminal, the data coder generating at the respective first and second data output terminals data read output signals having predetermined values when an active data mask control signal is applied to the data mask control terminal; and

an output stage having respective input terminals coupled to the first and second data output terminals of the data coder, the output stage generating the output data bit at data bit line that corresponds to the data read output signals from the data coder when the data read output signals do not have the predetermined values, the output stage producing a relatively high impedance at the data bit line when the data read output signals have the predetermined values.

71. The dynamic random access memory of claim 70 wherein the predetermined values of the data read output signals are any values in which the data read output signals at the respective data output terminals of the data coder have the same value.

72. The dynamic random access memory of claim 71 wherein the predetermined values of the data read output signal correspond to logic "1".

73. The dynamic random access memory of claim 70 wherein the data coder comprises:

a data mask register including the data mask control terminal, the data mask register receiving the data mask control signal on the data mask control terminal and a periodic clock signal on a clock input terminal, the register generating an output signal responsive to a predetermined portion of the clock signal after the data mask control signal becomes active; and

a data output register coupled to the data mask register and including the data input terminals and the data read output terminals, the data coder forcing the data read output signals to have the predetermined values responsive to the output signal from the data mask register.

74. The dynamic random access memory of claim 70 wherein the output stage comprises a logic circuit that causes the output data bit to have a first logic level responsive to one of the data read output signals having a first predetermined logic level, that causes the output data bit to have a second logic level responsive to the other of the data read output signals having a second predetermined logic level, and that causes the data bit line to have the relatively high impedance responsive to both of the read output signals having other than the first and second predetermined logic levels.

75. A computer system, comprising:

a processor having a processor data bus, address bus, and control bus;

an input device coupled to the processor;

an output device coupled to the processor;

a memory controller coupled to the processor; and

a dynamic random access memory having an address bus, at least one data bit line, and a plurality of control lines at least some of which are coupled to the memory controller, the dynamic random access memory comprising:

an array of memory cells having a plurality of memory cells, a plurality of row lines, a plurality of complimentary digit lines, and a pair of complimentary data ports;

a row address decoder coupled to the address bus, the row address decoder adapted to receive a row address on the address bus and activate a corresponding one of the row lines of the array;

a column address decoder coupled to the address bus, the column address decoder adapted to receive a column address on the address bus and couple a corresponding pair of complimentary digit lines of the array to respective data ports of the array; and

a data path coupled between the data ports and a data bit line, the data path including a input data buffer adapted to convert an input data bit applied to the data bit line to a corresponding input data signal and a complimentary input data signal, and to apply the input data signals to respective data ports of the array, and an output data buffer adapted to convert an output data signal and a complimentary output data signal applied to respective data ports of the array to an output data bit corresponding to the output data signal, and to apply the output data signal to the data bit line, the output buffer comprising:

a data coder having complimentary data input terminals coupled to the data ports of the array to receive respective output data signals, a pair of data output terminals, and a data mask control terminal, the data coder generating at respective first and second data output terminals complimentary data read output signals corresponding to complimentary data output signals applied to the respective input terminals of the data coder when an inactive data mask control signal is applied to the data mask control terminal, the data coder generating at the respective first and second data output terminals data read output signals having predetermined values when an active data mask control signal is applied to the data mask control terminal; and

an output stage having respective input terminals coupled to the first and second data output terminals of the data coder, the output stage generating the output data bit at data bit line that corresponds to the data read output signals from

the data coder when the data read output signals do not have the predetermined values, the output stage producing a relatively high impedance at the data bit line when the data read output signals have the predetermined values.

76. The computer system of claim 75 wherein the predetermined values of the data read output signals are any values in which the data read output signals at the respective data output terminals of the data coder have the same value.

77. The computer system of claim 76 wherein the predetermined values of the data read output signal correspond to logic "1".

78. The computer system of claim 75 wherein the output stage comprises a logic circuit that causes the output data bit to have a first logic level responsive to one of the data read output signals having a first predetermined logic level, that causes the output data bit to have a second logic level responsive to the other of the data read output signals having a second predetermined logic level, and that causes the data bit line to have the relatively high impedance responsive to both of the read output signals having other than the first and second predetermined logic levels. - -

REMARKS

Consideration of this reissue application in view of the above amendments and following remarks is respectfully requested. Applicant is requesting reissue on the basis that the '314 patent is, through error without any deceptive intention, deemed wholly or partially inoperative by reason of the patentee claiming less than he had a right to claim in the '314 patent. The assignee offers to surrender the '314 patent once the Examiner has indicated the allowability of all claims associated with this reissue application. The assignee is requesting a reissue of the '314 patent for the invention as disclosed in the '314 patent and claimed in issued claims 1-53 and new claims 54-78.

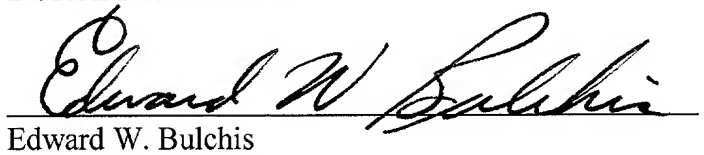
No new matter has been introduced into this application for reissue.

Applicant believes claims 1-78 are in condition for allowance and respectfully requests such action.

If there are any matters that can be handled in a telephone conversation, the Examiner is encouraged to contact Mr. Bulchis at (206) 903-8785.

Respectfully submitted,

DORSEY & WHITNEY LLP



Edward W. Bulchis
Registration No. 26,847

EWB:mp

1420 Fifth Avenue, Suite 3400
Seattle, Washington 98101-4010
(206) 903-8800
Fax: (206) 903-8820

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